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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/003,434	12/06/2001	Nobuyo Sugiyama	60188-127	7445

7590 12/18/2002

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EXAMINER
QUINTO, KEVIN V

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 12/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/003,434	Applicant(s) SUGIYAMA ET AL.
	Examiner Kevin Quinto	Art Unit 2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 September 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) *13-21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6,10 and 11* is/are rejected.

7)☒ Claim(s) *5,7-9 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Claims 13-21 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 6.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

3. Claims 3-5 are objected to because of the following informalities: the use of the term "embedded region adjacent upper area" in these claims. The examiner believes that this term is grammatically incorrect. Appropriate correction is required.

4. Claims 7 and 8 are objected to because of the following informalities: the use of the term "embedded region adjacent lower area" in these claims. The examiner believes that this term is grammatically incorrect. Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Sedra and Smith, "Microelectronic Circuits," p.968-970.

7. In reference to claim 1, Sedra and Smith ("Microelectronic Circuits," p.968-970, hereinafter referred to as the "Sedra" reference) discloses a similar device. On p. 969 of Sedra, figure 13-46 illustrates a nonvolatile semiconductor memory device with a floating gate electrode, formed on a semiconductor region, for storing carriers injected from said semiconductor region. There is a select gate or control gate for controlling a quantity of stored carriers by applying a predetermined voltage to the floating gate electrode. There is a source region in the semiconductor region on one side of the floating gate and the control gate. There is a drain region in the semiconductor region on the other side of the floating gate and the control gate. During programming, the drain region creates an electric field so that the carriers injected into the floating gate are subject to an external force having an element directed from the semiconductor region to the floating gate.

8. Claims 1, 2, 10, and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Mizutani (USPN 4,665,418).

9. In reference to claim 1, Mizutani (USPN 4,665,418, hereinafter referred to as the "Mizutani" reference) discloses a similar device. Figure 6 of Mizutani illustrates a nonvolatile semiconductor memory device with a floating gate electrode (15), formed on a semiconductor region, for storing carriers injected from said semiconductor region. There is a control gate (17) for controlling a quantity of stored carriers by applying a predetermined voltage to the floating

gate electrode (15). There is a source region (11) in the semiconductor region on one side of the floating gate (15) and the control gate (17). There is a drain region (20, 21) in the semiconductor region on the other side of the floating gate (15) and the control gate (17). Although the Mizutani device utilizes a source side injection method of operation, the drain region (20, 21) does create an electric field so that the carriers injected into the floating gate (15) are subject to an external force having an element directed from the semiconductor region to the floating gate (15).

10. In reference to claim 2, Mizutani discloses a similar device. Figure 6 of Mizutani illustrates a nonvolatile semiconductor memory device with a floating gate (15) formed on a semiconductor region via a first dielectric film (16). There is a control gate (17) capacitively coupled with the floating gate (15) via a second dielectric film (not labeled). There is a source region (11) and a drain region (20) formed in the semiconductor region on side regions of the floating gate (15) and the control gate (17). The end of the drain region (20) facing the source region has an embedded drain region (21). It is understood that a channel is formed near the surface of the semiconductor region above the embedded drain region (21).

11. In reference to claim 10, the device of Mizutani inherently meets this limitation. Carriers located in the channel region under the floating gate are subject to a force element of the electric field perpendicular to the surface of said semiconductor region when a predetermined voltage is applied to the control gate. This operation is explained in column 4, lines 63-68 and column 5, lines 1-20.

12. With regard to claim 11, the control gate (17) is above the floating gate (15).

13. Claims 2, 10, and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Kaya et al. (USPN 5,264,384).

14. In reference to claim 2, Kaya et al. (USPN 5,264,384, hereinafter referred to as the "Kaya" reference) discloses a similar device. Figure 10e of Kaya illustrates a nonvolatile semiconductor memory device with a floating gate (13) formed on a semiconductor region via a first dielectric film (22). There is a control gate (14) capacitively coupled with the floating gate (13) via a second dielectric film (23). There is a source region (11) and a drain region (12) formed in the semiconductor region on side regions of the floating gate (13) and the control gate (14). The end of the drain region (12) facing the source region has an embedded drain region (not labeled, but shown more clearly in figure 10b). It is understood that a channel is formed near the surface of the semiconductor region above the embedded drain region.

15. In reference to claim 10, the device of Kaya inherently meets this limitation. Carriers located in the channel region under the floating gate are subject to a force element of the electric field perpendicular to the surface of said semiconductor region when a predetermined voltage is applied to the control gate. This operation is explained in column 1, lines 39-47.

16. With regard to claim 11, the control gate (14) is above the floating gate (13).

17. Claims 1, 2, 10, and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Burr et al. (USPN 5,780,912).

18. In reference to claim 1, Burr et al. (USPN 5,780,912, hereinafter referred to as the "Burr" reference) discloses a similar device. Figure 3 of Burr illustrates a nonvolatile semiconductor memory device with a floating gate electrode (54), formed on a semiconductor region, for storing carriers injected from said semiconductor region. There is a select gate or control gate (56) for

controlling a quantity of stored carriers by applying a predetermined voltage to the floating gate electrode (54). There is a source region (36') in the semiconductor region on one side of the floating gate (54) and the control gate (56). There is a drain region (38') in the semiconductor region on the other side of the floating gate (54) and the control gate (56). During programming, the drain region (38') creates an electric field so that the carriers injected into the floating gate (54) are subject to an external force having an element directed from the semiconductor region to the floating gate (54). This operation is described by Sedra and Smith, "Microelectronic Circuits," p.968-970.

19. In reference to claim 2, Burr discloses a similar device. Figure 3 of Burr illustrates a nonvolatile semiconductor memory device with a floating gate (54) formed on a semiconductor region via a first dielectric film (40'). There is a control gate (56) capacitively coupled with the floating gate (54) via a second dielectric film (not labeled). There is a source region (36') and a drain region (38') formed in the semiconductor region on side regions of the floating gate (54) and the control gate (56). Although figure 3 shows that there is an embedded impurity region (47') on the source side, Burr makes it clear that this embedded impurity region (47') may also be on the drain side (abstract and claim 1). It is understood that a channel is formed near the surface of the semiconductor region above the embedded impurity region (47').

20. In reference to claim 10, the device of Burr inherently meets this limitation. During programming, the source is held to ground while a voltage is applied to the drain. Carriers located in the channel region under the floating gate are subject to a force element of the electric field perpendicular to the surface of said semiconductor region when a predetermined voltage is

applied to the control gate or the drain. This operation is described by Sedra and Smith, "Microelectronic Circuits," p.968-970.

21. With regard to claim 11, the control gate (56) is above the floating gate (54).

22. Claims 1-4, 6, 10, and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Hori et al. (Published Japanese Application, Publication No.: JP 11-345888).

23. In reference to claim 1, Hori et al. (Published Japanese Application, Publication No.: JP 11-345888, hereinafter referred to as the "Hori" reference) discloses a similar device. Disclosed with this Office action is a machine translation generated by the Japanese Patent Office website; however a full translation is pending. Figure 14 of Hori illustrates a nonvolatile semiconductor memory device with a floating gate electrode (3), formed on a semiconductor region (1), for storing carriers injected from said semiconductor region (1). There is a control gate (5) for controlling a quantity of stored carriers by applying a predetermined voltage to the floating gate electrode (3). There is a source region (11a) in the semiconductor region (1) on one side of the floating gate (3) and the control gate (5). There is a drain region (11b) in the semiconductor region (1) on the other side of the floating gate (3) and the control gate (5). During programming, the drain region (11b) creates an electric field so that the carriers injected into the floating gate (3) are subject to an external force having an element directed from the semiconductor region (1) to the floating gate (3). This operation is described by Sedra and Smith, "Microelectronic Circuits," p.968-970.

24. In reference to claim 2, Hori discloses a similar device. Figure 14 of Hori illustrates a nonvolatile semiconductor memory device with a floating gate (3) formed on a semiconductor region (1) via a first dielectric film (2). There is a control gate (5) capacitively coupled with the

floating gate (3) via a second dielectric film (4). There is a source region (11a) and a drain region (11b) formed in the semiconductor region (1) on side regions of the floating gate (3) and the control gate (5). The end of the drain region (11b) facing the source region (11a) has an embedded drain region (12b). It is understood that a channel is formed near the surface of the semiconductor region (1) above the embedded drain region (12b).

25. With regard to claim 3, there is an embedded region adjacent upper area (7b) that is formed in an upper part of said embedded drain region (12b) in the semiconductor region and has a conduction type (p-type) opposite to that of the drain region (11b, n-type).

26. In reference to claim 4, the embedded region adjacent upper area (7b) has a concentration of 1×10^{17} to 1×10^{18} cm^{-3} (paragraph 148) while the semiconductor region (1) has a concentration of 5×10^{15} to 5×10^{16} cm^{-3} (paragraph 47).

27. With regard to claim 6, figure 14 shows that the embedded drain region (12b) has the same conduction type as that of the drain region (11b). The impurity concentration of the embedded drain (12b) is lower than the impurity concentration of the drain (11b).

28. In reference to claim 10, the device of Hori inherently meets this limitation. The solution section of Hori makes it clear that the electric field is maximized at the drain side of the device during write mode. Thus carriers located in the channel region under the floating gate are subject to a force element of the electric field perpendicular to the surface of said semiconductor region when a predetermined voltage is applied to the control gate or the drain.

29. With regard to claim 11, the control gate (5) is above the floating gate (3).

Allowable Subject Matter

30. Claims 5, 7-9, and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

31. The following is a statement of reasons for the indication of allowable subject matter: the examiner is unaware of a nonvolatile semiconductor memory device with an embedded drain (below the top surface of the substrate) with a lower portion or an embedded drain (below the top surface of the substrate and having conductivity type opposite to that of the drain) with an upper portion.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (703) 306-5688. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

KVQ
December 9, 2002

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